

# RS780Q-LAIO MXM

VER:1.2

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### PCB STACK:

L1:TOP  
L2:PWR  
L3:INT1  
L4:INT2  
L5:GND  
L6:BOTTOM

6 Layer Stackup	
SOLDERMASK	0.6 mil
L1 Signal	1.55 mil
PP 2116	4.65 mil
L2 POWER	1.3 mil
0.127mm(不含銅厚)	5 mil
L3 Signal 10Z	1.3 mil
0.864mm無銅基板	34 mil
L4 Signal 10Z	1.3 mil
0.127mm(不含銅厚)	5 mil
L5 GND 10Z	1.3 mil
PP 2116	4.65 mil
L6 Signal	1.55 mil
SOLDERMASK	0.6 mil
Total Board Thickness	62.8 mil

## SB710 GPIO Function

[illegible]

## IT8720 GPIO

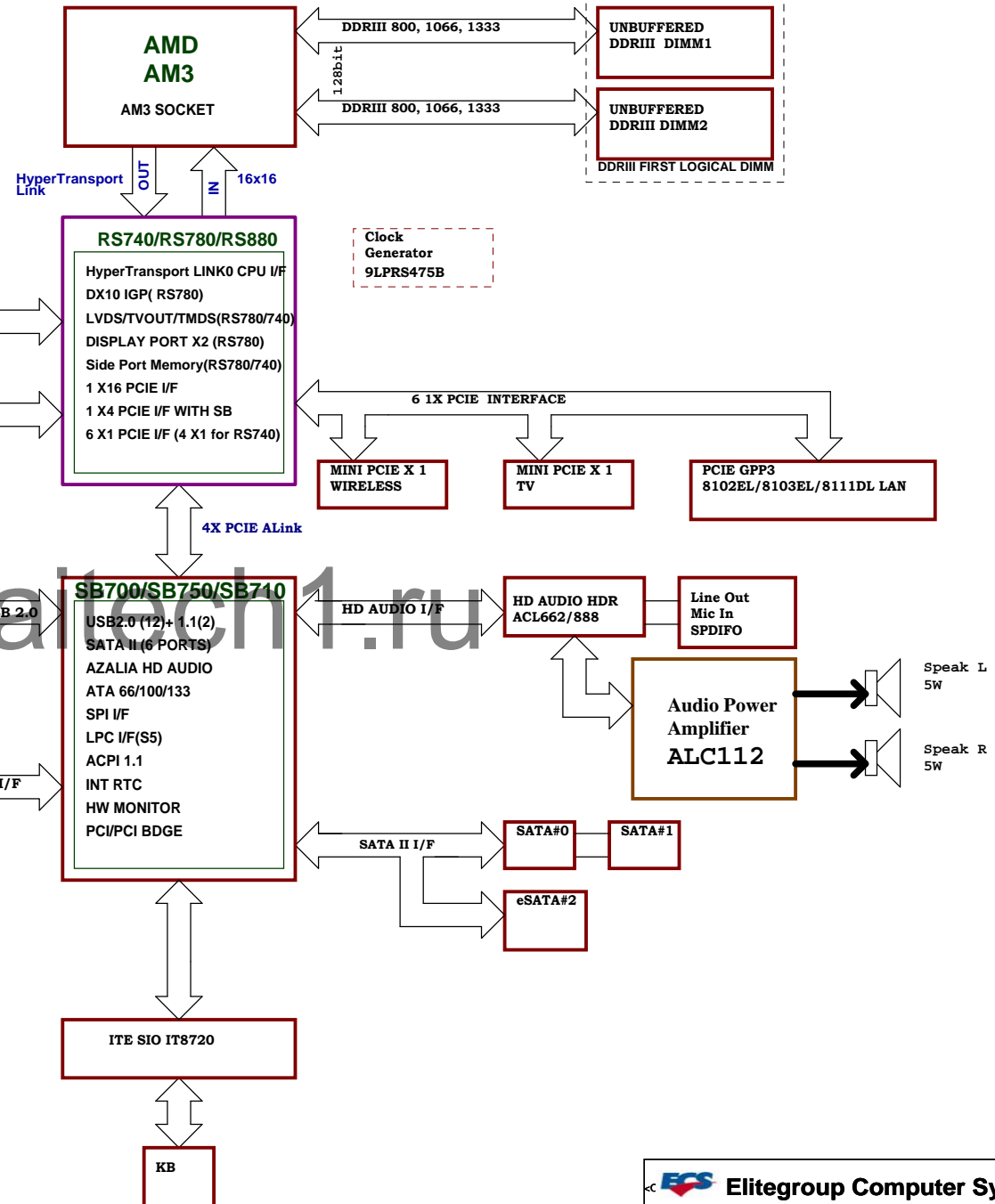
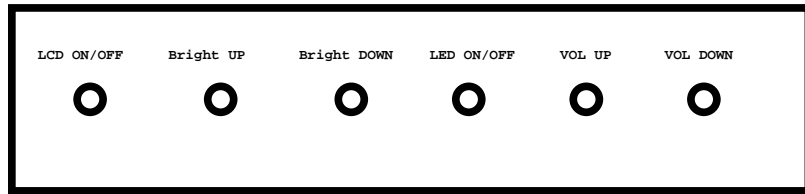
Signal Name	Type	Voltage	Default	Functional Description	Net name
GP14	I/O	5V	GPI	Reserve	GP14
GP21	I/O	5VSB	GPI	MXM full power or reduce power Control	MXM_PWR_LEVEL
GP22	I/O	5VSB	GPI	Power LED Control	LED0
GP23	I/O	5VSB	GPI	Power LED Control	LED1
GP27	I/O	5VSB	GPI	MXM module present detect	MXM_PRSENT1-
GP30	I/O	5V	GPI	For BUZZER Control	BEEP
GP31	I/O	5V	GPI	Disables RF portion of the MiniCard	WLAN_DIS-
GP32	I/O	5V	GPI	Thermal trip	THRM_L
GP33	I/O	5V	GPI	Disables TV portion of the MiniCard	TVCARD_DIS-
GP34	I/O	5V	GPI	Reserve	GP34
GP35	I/O	5V	GPI	For TOP,LEFT,RIGHT LED Control	LED_BOARD
GP36	I/O	5V	GPI	adjust PWM for LCD brightness +/-	BL_ADJ_SIO
GP37	I/O	5V	GPI	Control Inverter on/ff	INVERTER_EN
GP40	I/O	5VSB	GPI	DIMM DUAL Control	GP40
GP46	I/O	5VSB	GPO	LAN WAKEUP Disable	WAKEUP
GP50	I/O	5V	GPI	Reserve	GP50
GP80	I/O	5V	GPI	AMP_GAIN1	AMP_GAIN1
GP81	I/O	5V	GPI	AMP_GAIN0	AMP_GAIN0
GP82	I/O	5V	GPI	Thermal interrupt request	MXM_ALERT
GP84	I/O	5V	GPI	Thermal shutdown request	MXM_OVERT

<i>Job</i>	<i>Signature</i>	<i>Date</i>
<b><i>Schematics Designer</i></b>		
<b><i>Layout</i></b>		
<b><i>Approval</i></b>		

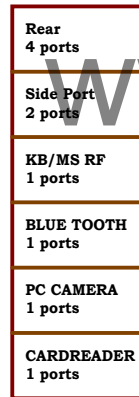
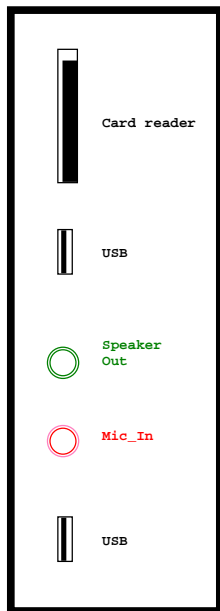
 <b>Elitegroup Computer Systems</b>			
<b>COVER PAGE</b>			
Title			
Size	Document Number		Rev
Custom	<b>RS780Q-LAIO</b>		<b>1.2</b>
Date:	Friday, August 14, 2009		Sheet 1 of 26

# RS780Q-LAIO

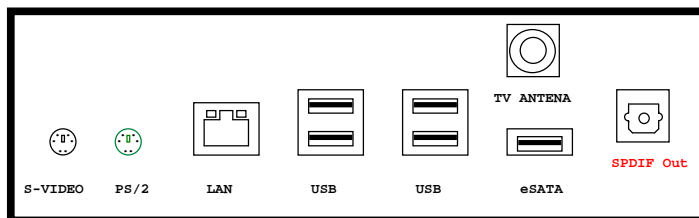
## FRONT TOUCH SENSOR



## SIDE IO

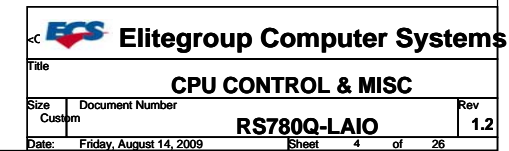


## Rear IO HEADER 64 Pin

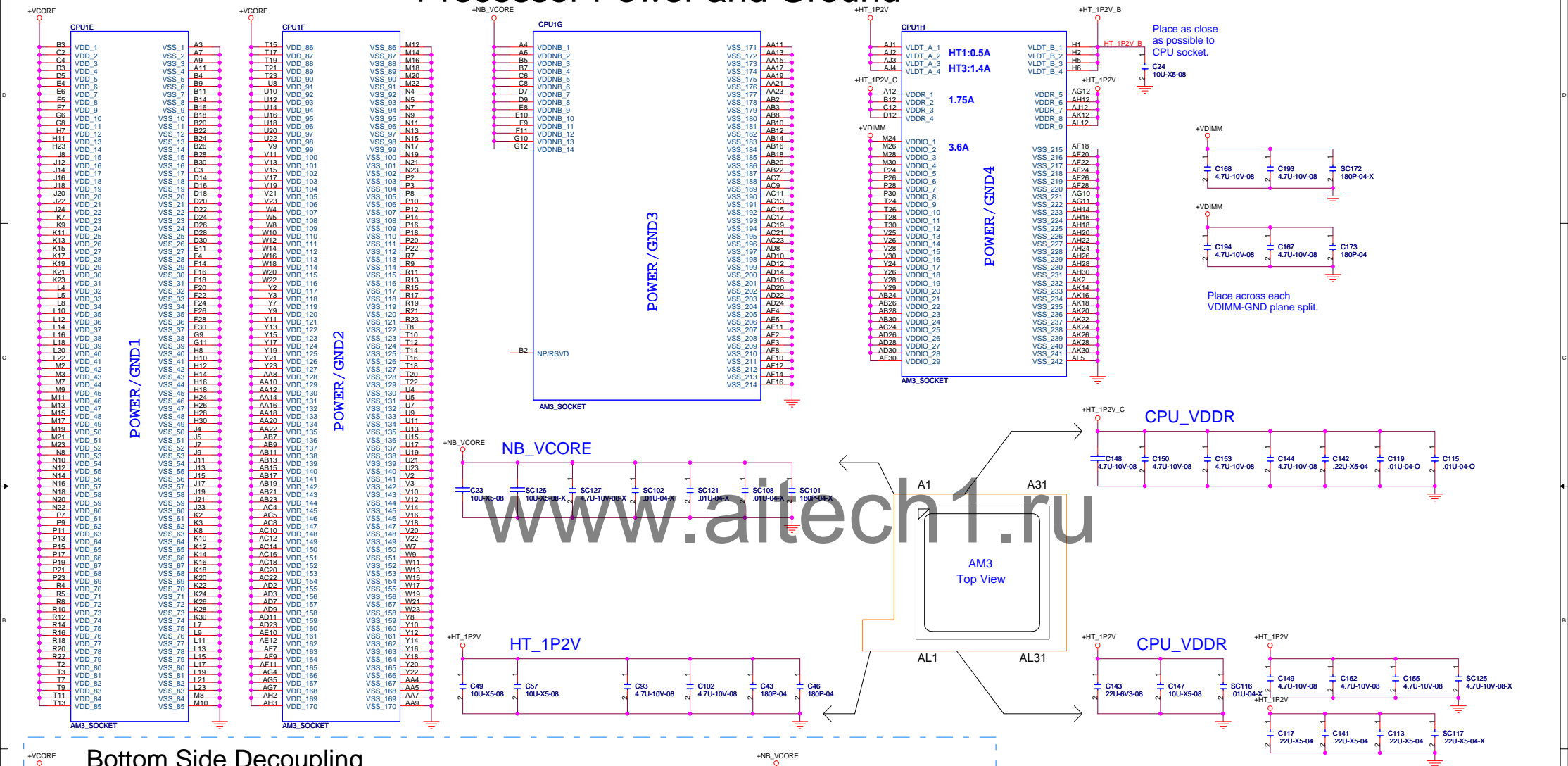




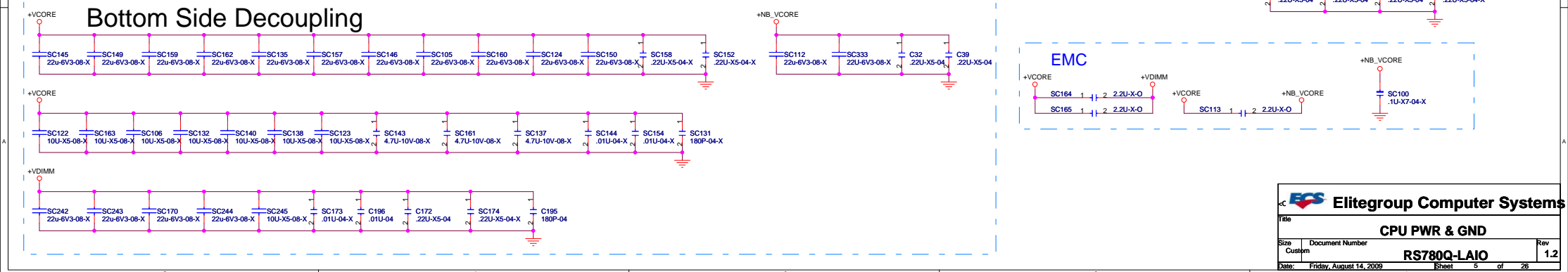
## CPU Control and Miscellaneous

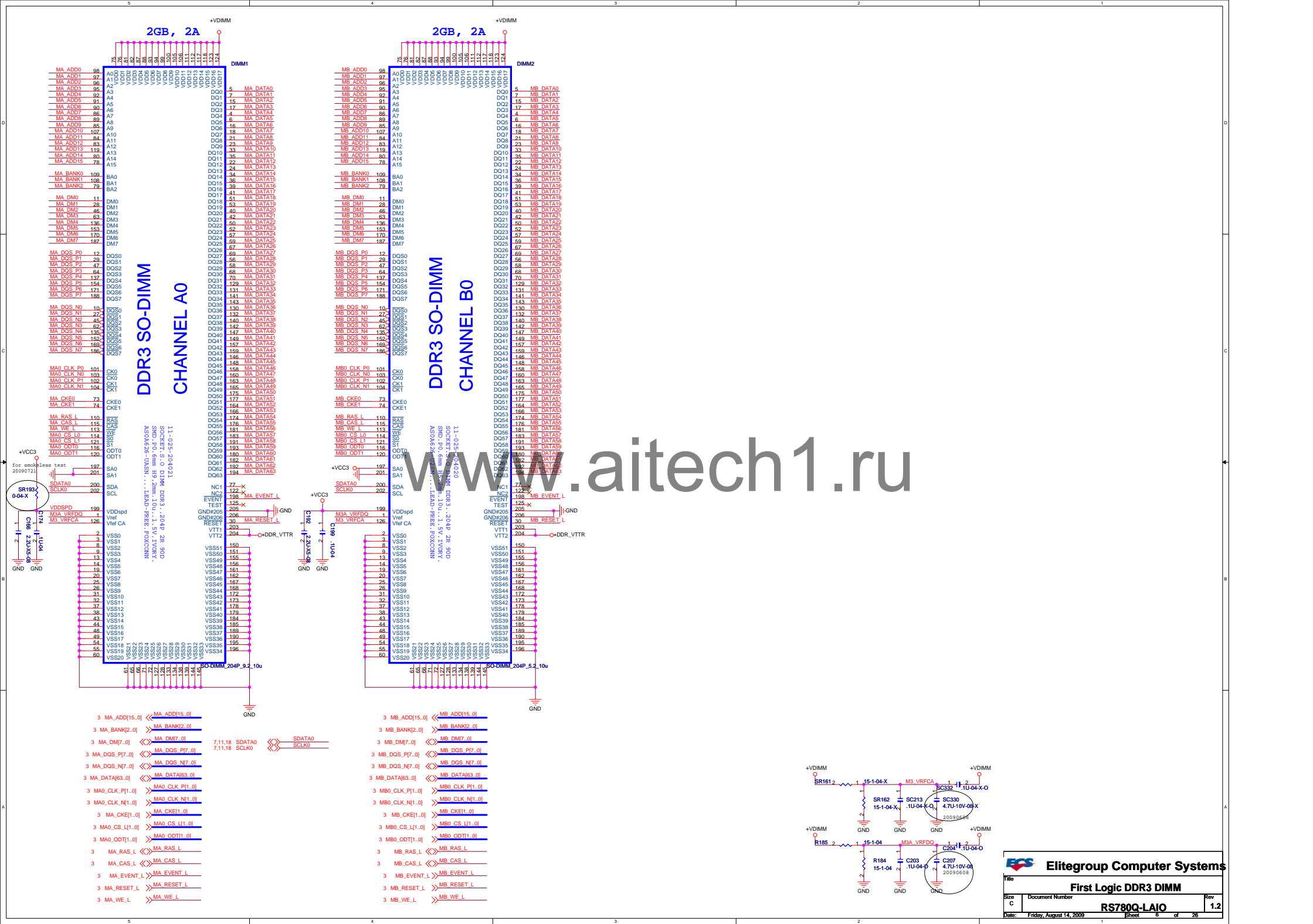


# Processor Power and Ground

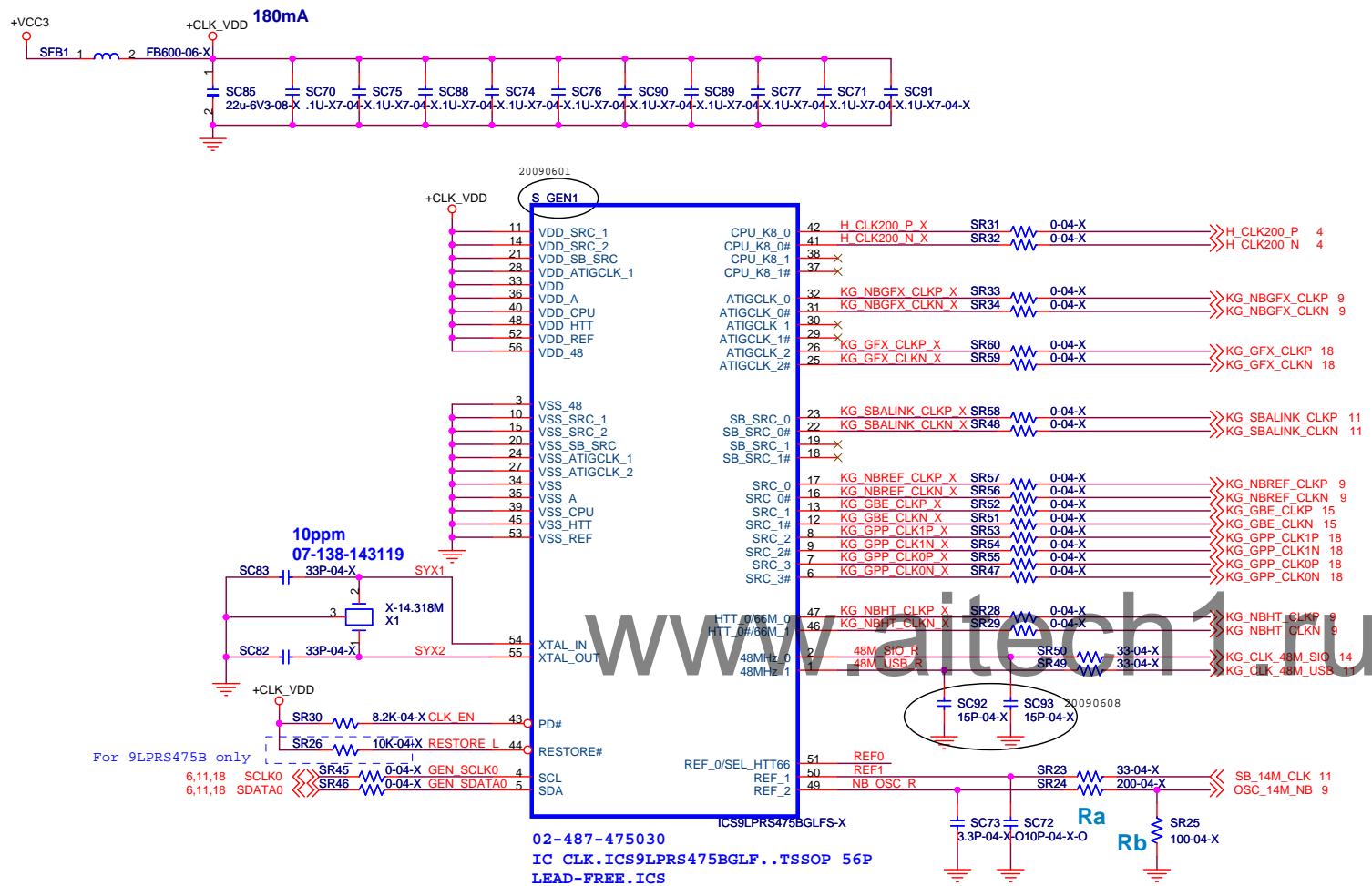


## Bottom Side Decoupling









## PART 1 OF 6

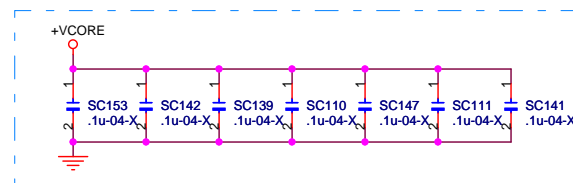
## HYPER TRANSPORT CPU I/F



RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RS780
HT_RXCALP	49.9R (GND)	
HT_RXCALN	49.9R (VDDHT)	301
HT_TXCALP		
HT_TXCALN	100R	301

## HT LINK STITCHING CAPS.



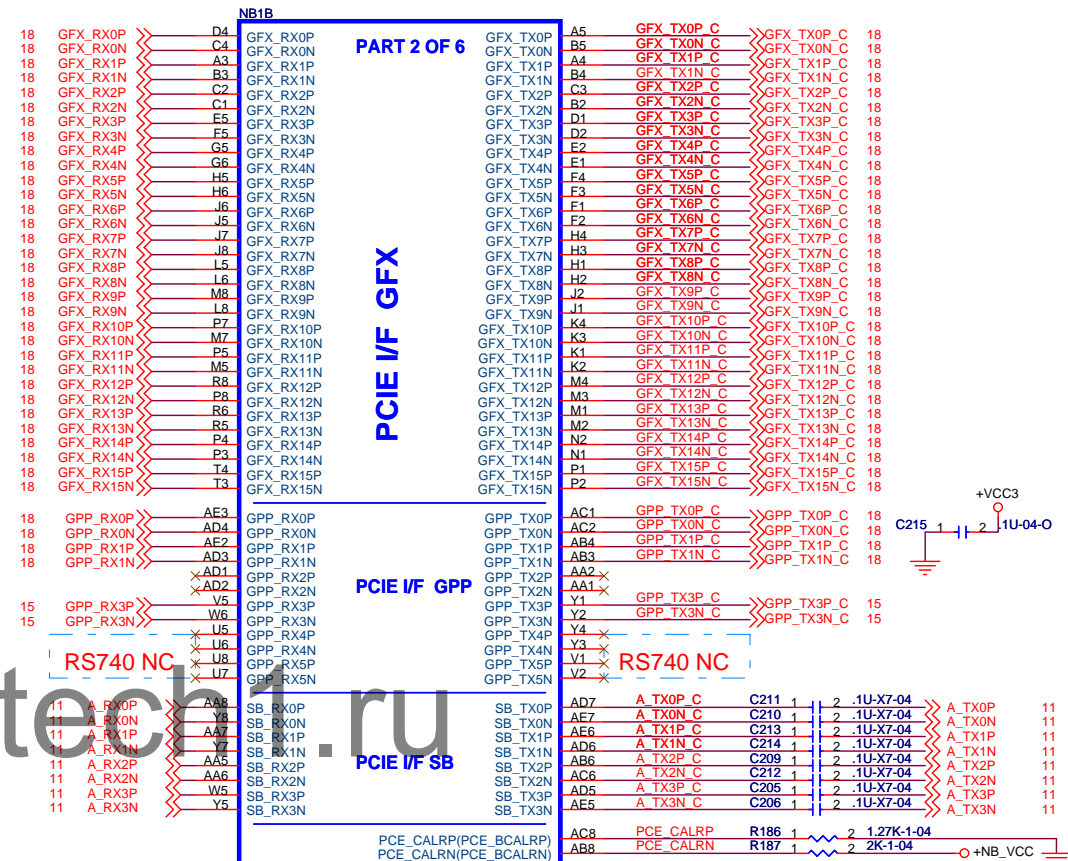
3 H\_CADOUT\_P[15..0] >> H\_CADOUT\_P[15..0]  
 3 H\_CADOUT\_N[15..0] >> H\_CADOUT\_N[15..0]  
 3 H\_CLKOUT\_P[1..0] >> H\_CLKOUT\_P[1..0]  
 3 H\_CLKOUT\_N[1..0] >> H\_CLKOUT\_N[1..0]  
 3 H\_CTLOUT\_P[1..0] >> H\_CTLOUT\_P[1..0]  
 3 H\_CTLOUT\_N[1..0] >> H\_CTLOUT\_N[1..0]  
 3 H\_CADIN\_P[15..0] >> H\_CADIN\_P[15..0]  
 3 H\_CADIN\_N[15..0] >> H\_CADIN\_N[15..0]  
 3 H\_CLKIN\_P[1..0] >> H\_CLKIN\_P[1..0]  
 3 H\_CLKIN\_N[1..0] >> H\_CLKIN\_N[1..0]  
 3 H\_CTLIN\_P[1..0] >> H\_CTLIN\_P[1..0]  
 3 H\_CTLIN\_N[1..0] >> H\_CTLIN\_N[1..0]

## PART 2 OF 6

## PCI-E I/F GFX

## PCI-E I/F GPP

## PCI-E I/F SB

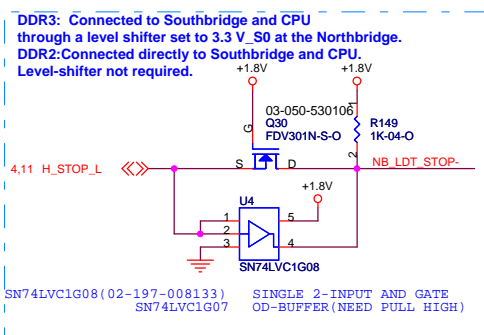
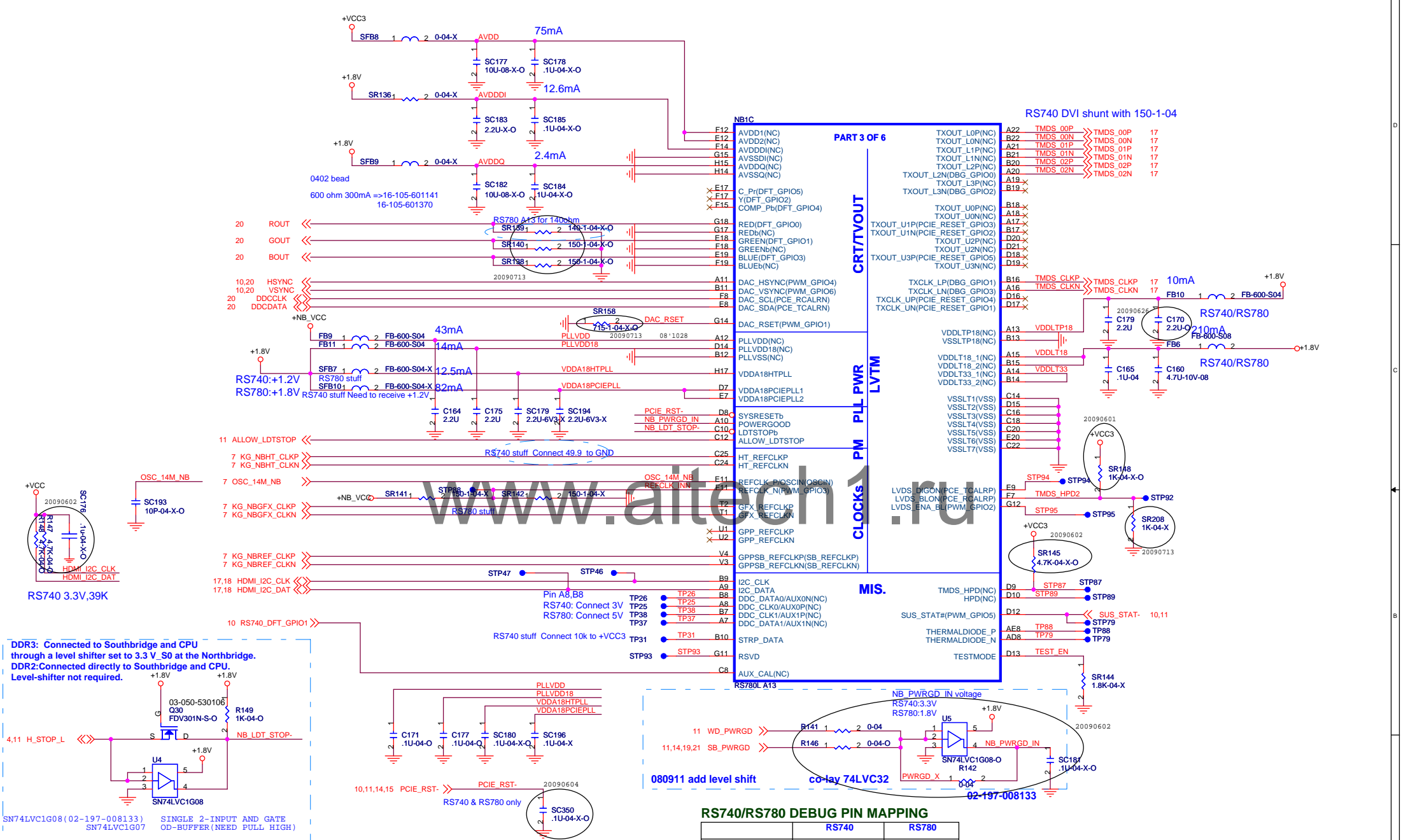


RS780L A13

01-201-215123

IC CHIP:RS780L(215-0674042) A13.  
 (BUY-LENOVO).FCBGA 528P.....  
 LEAD-FREE (RoHS) .AMD





**RS740/RS780 difference table (Control signal)**

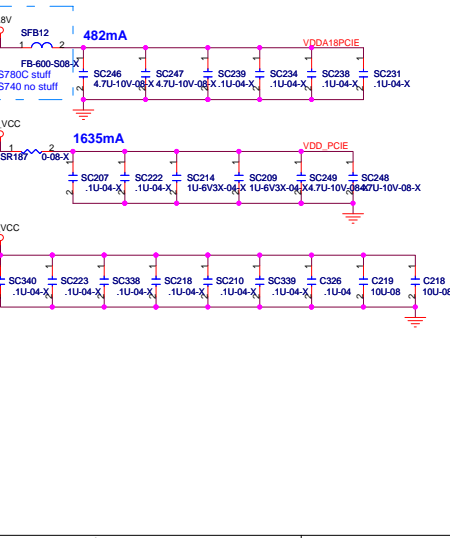
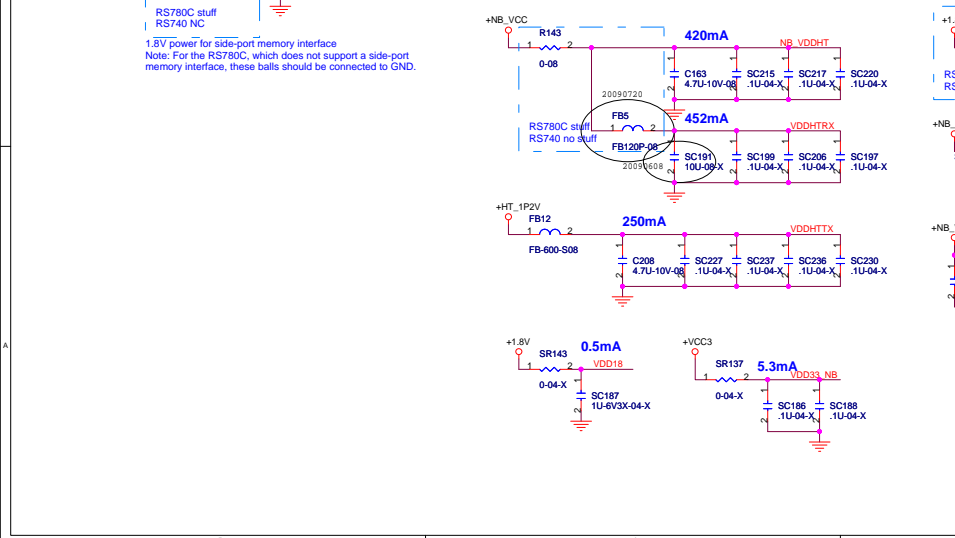
	RS740	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN
ALLOW_LDTSTOP	OD	OD/3.3V IN
H_STOP_L	3.3V IN	3.3V IN/OD
IN(default)/OUT	3.3V IN	3.3V IN
SYSTEMRESETB	3.3V IN	3.3V IN

**RS740/RS780 JTAG PIN MAPPING**

	RS740/RS780
TRST	TEST_EN
TMS(TP220)	DDC_DATA(TP223)
TDI	I2C_DATA
TCK	I2C_CLK
TDO(TP218)	TMDS_HPD(TP221)

**RS740/RS780 DEBUG PIN MAPPING**

	RS740	RS780
DEBUG_OUT0	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	X	AUX1N
DEBUG_OUT5	X	AUX1P
DEBUG_OUT6	X	HPD
DEBUG_OUT7	X	AUX_CAL



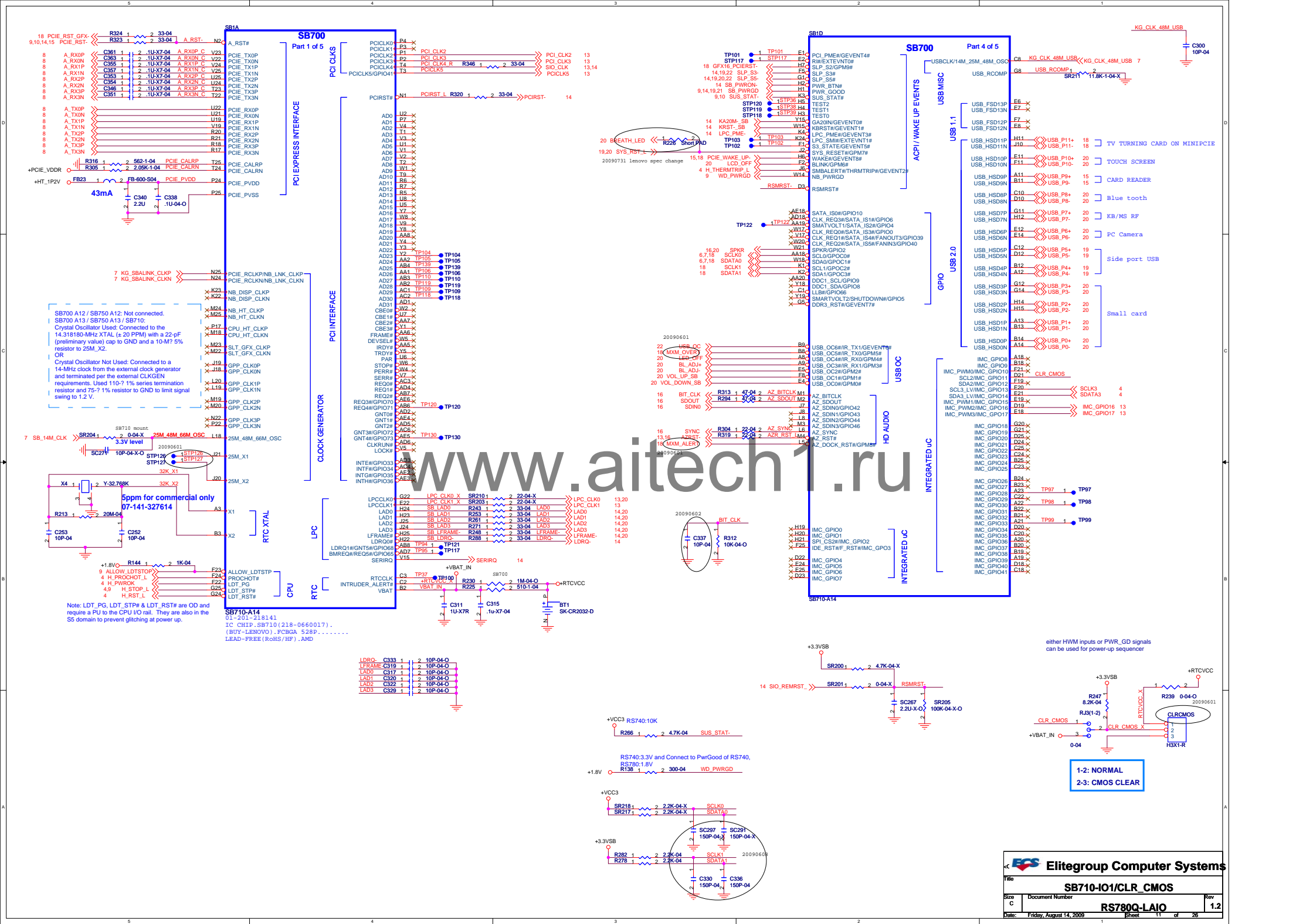
Enables Test debug bus using PCIe bus

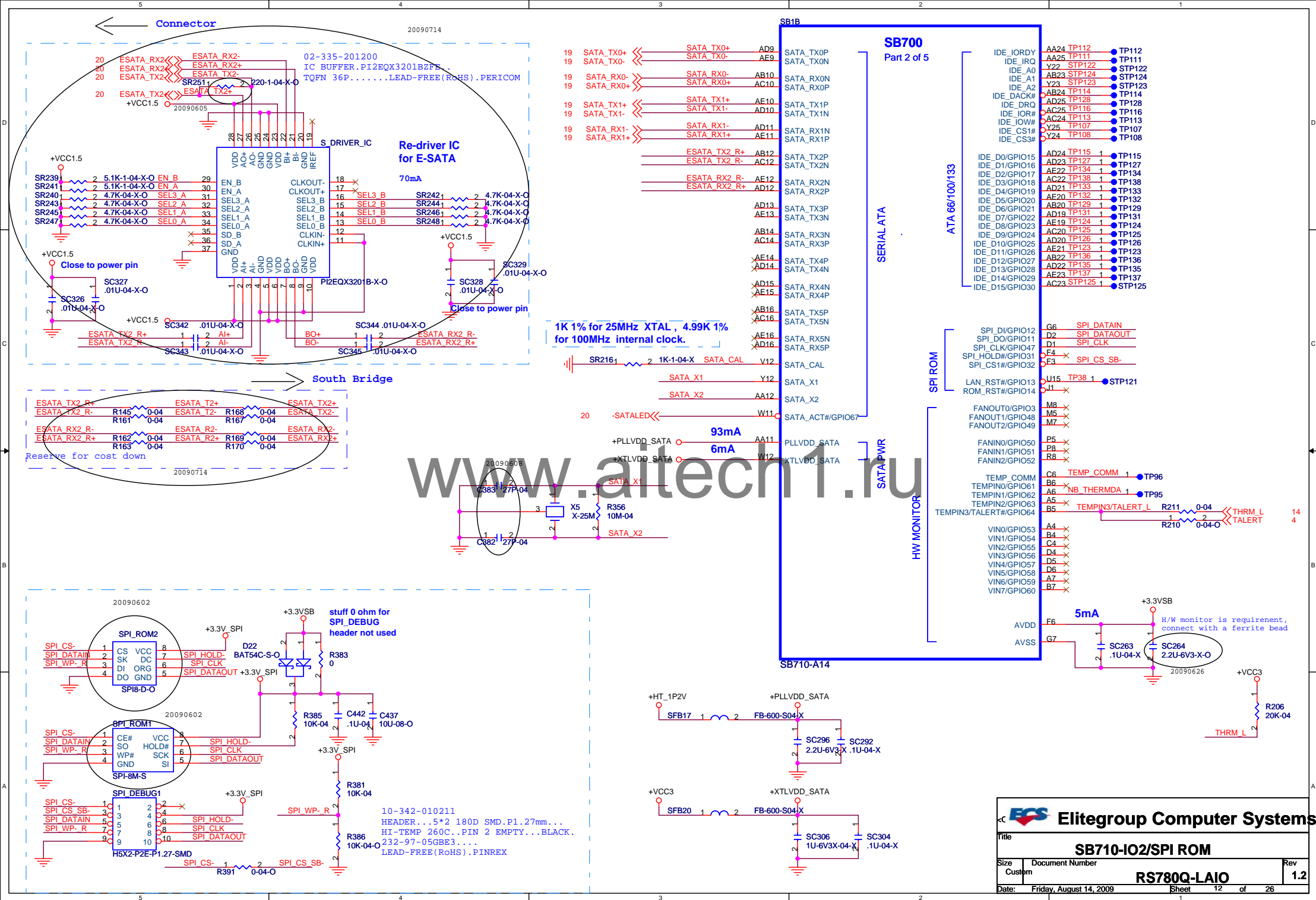
1. Disable (can be enabled thru nbcfg register)

0 : Enable

RS780: configurable thru register setting only

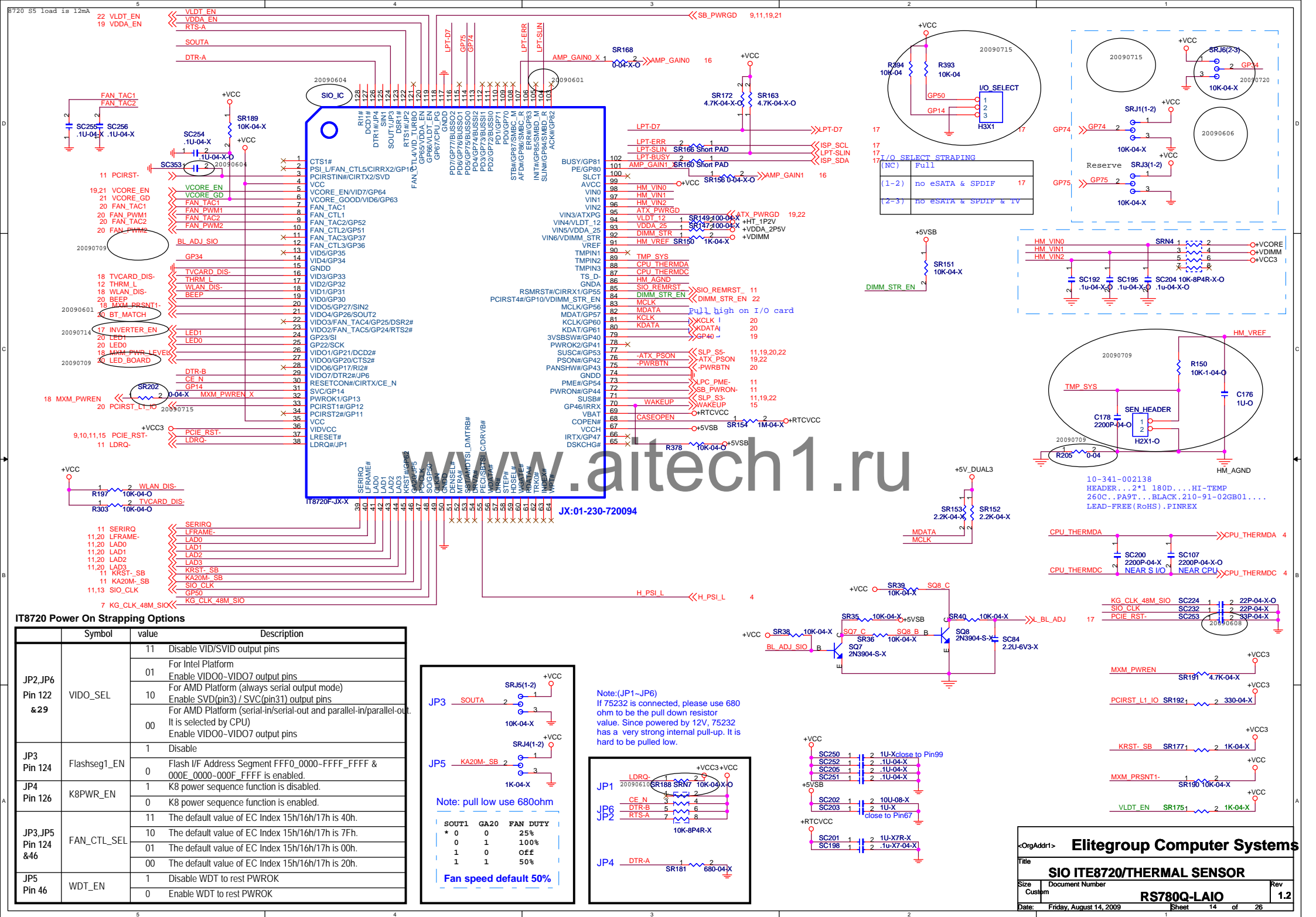
PIN NAME	RS740	RS780	PIN NAME	RS740	RS780
VDDHT	NC	+1.1V	IOPLLVDD	+1.2V	+1.1V
VDDHTRX	NC	+1.1V	AVDD	+3.3V	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	+1.8V	+1.8V
VDDA18P0CIE	NC	+1.8V	AVDDQ	+1.8V	+1.8V
VDDI18	+1.8V	+1.8V	PLLVDD	+1.2V	+1.1V
VDDI18_MEM	NC	+1.8V	PLLVDDI18	+1.8V	+1.8V
VDDP0CIE	+1.2V	+1.1V	VDDA18P0CIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	VDDA18HTPLLL	+1.8V	+1.8V
VDD_MEM	+1.8V	+1.8V(DDR2) +1.6V(DDR3)	VDDLTPI18	+1.8V	+1.8V
VDD33	+3.3V	+3.3V	VDDLT18	+1.8V	+1.8V
IOPLLVDDI18	+1.8V	+1.8V	VDDLT33	+3.3V	NC





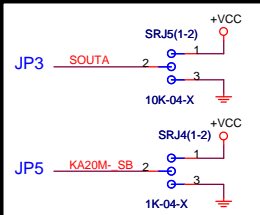






IT8720 Power On Strapping Options

	Symbol	value	Description
JP2,JP6 Pin 122 &29	VIDO_SEL	11	Disable VID/SVID output pins
		01	For Intel Platform Enable VIDO0~VIDO7 output pins
		10	For AMD Platform (always serial output mode) Enable SVD(pin3) / SVC(pin31) output pins
		00	For AMD Platform (serial-in/serial-out and parallel-in/parallel-out) It is selected by CPU) Enable VIDO0~VIDO7 output pins
JP3 Pin 124	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment FFF0_0000~FFFF_FFFF & 000E_0000~000F_FFFF is enabled.
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled.
		0	K8 power sequence function is enabled.
JP3,JP5 Pin 124 &46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h.
		10	The default value of EC Index 15h/16h/17h is 7Fh.
		01	The default value of EC Index 15h/16h/17h is 00h.
		00	The default value of EC Index 15h/16h/17h is 20h.
JP5 Pin 46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

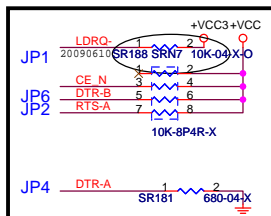


Note: pull low use 680ohm

SOUT1	GA20	FAN	DUTY
* 0	0	25%	
0	1	100%	
1	0	00%	
1	1	50%	

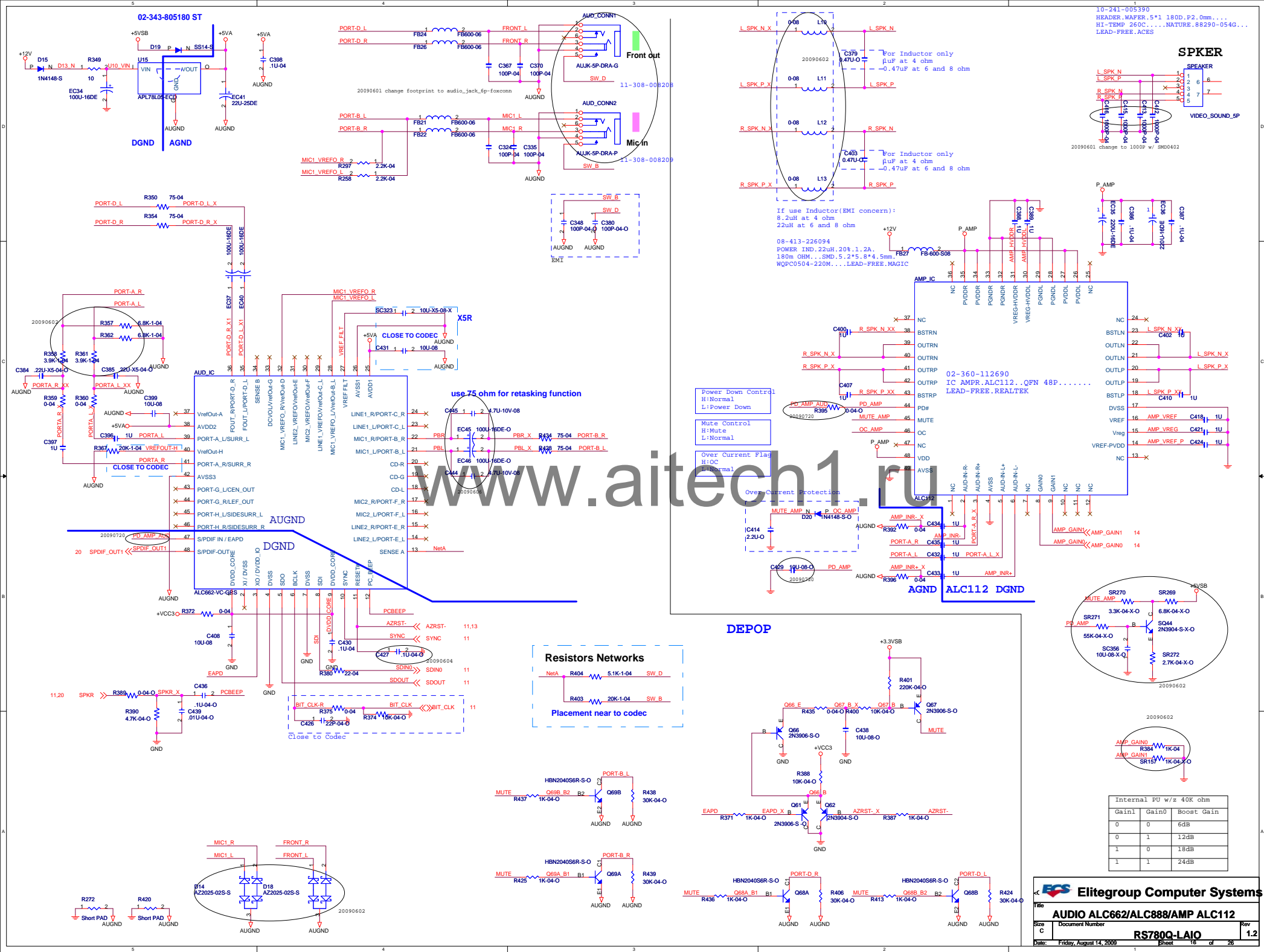
Fan speed default 50%

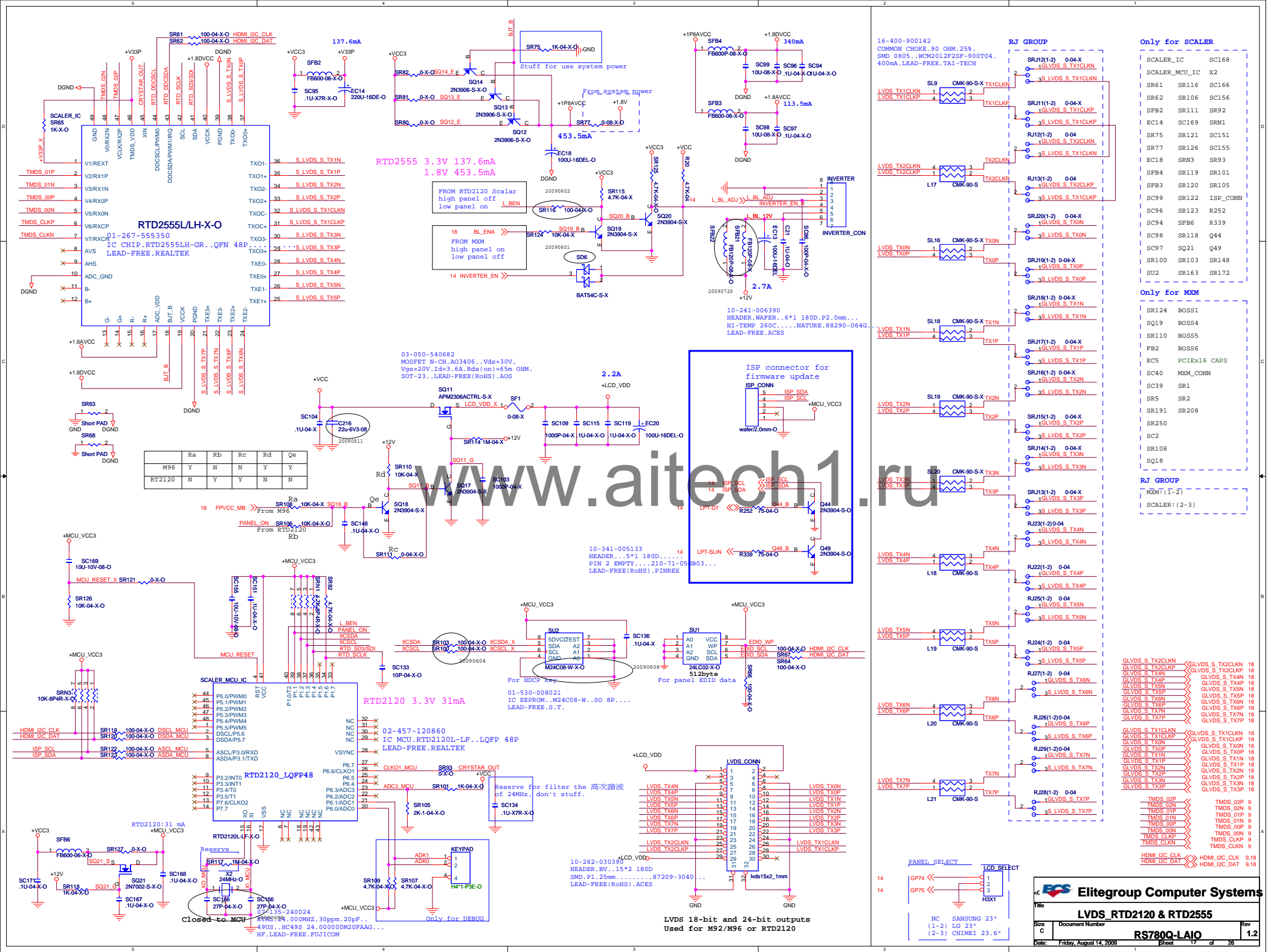
Note: (JP1~JP6)  
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low.

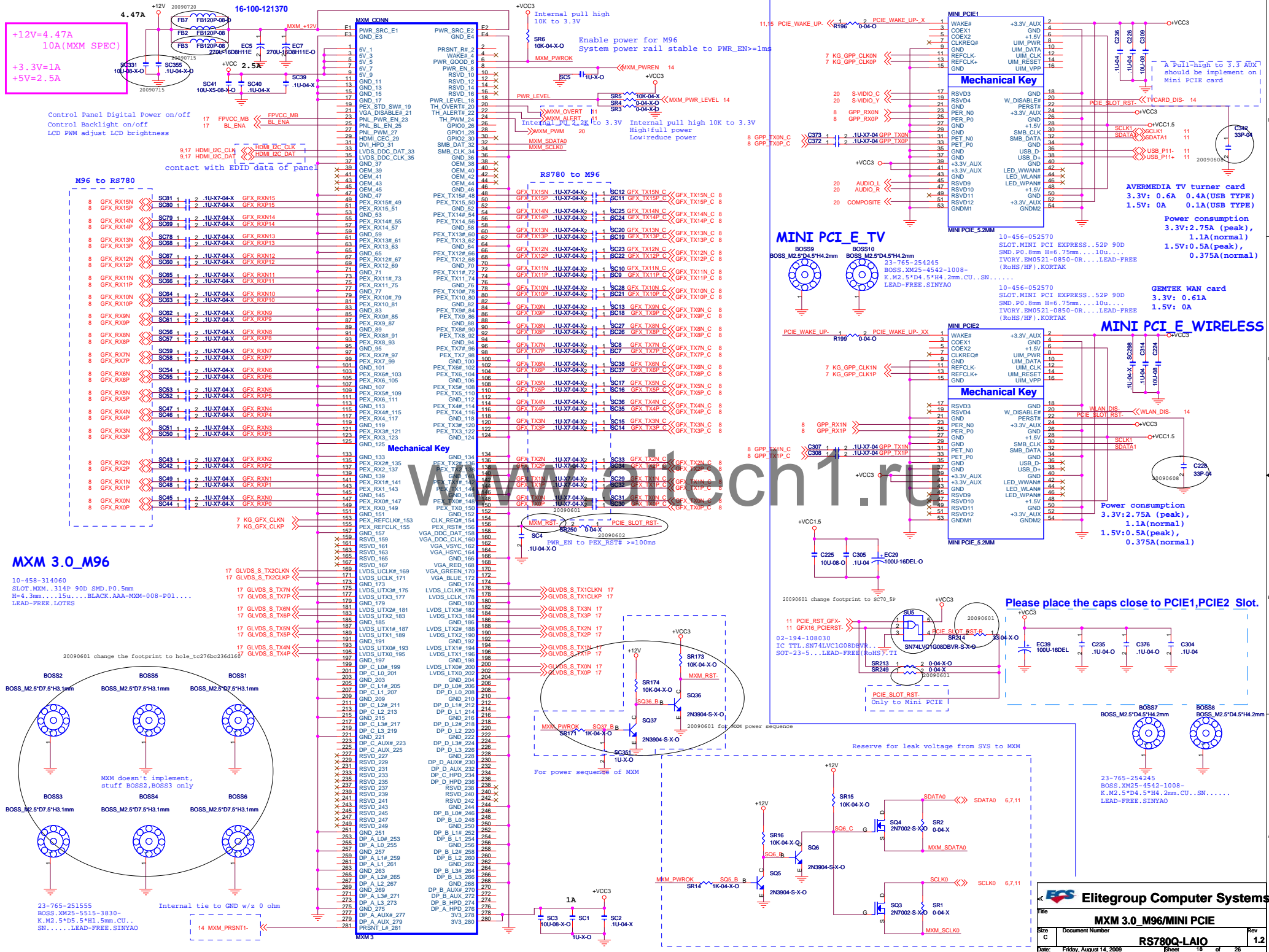






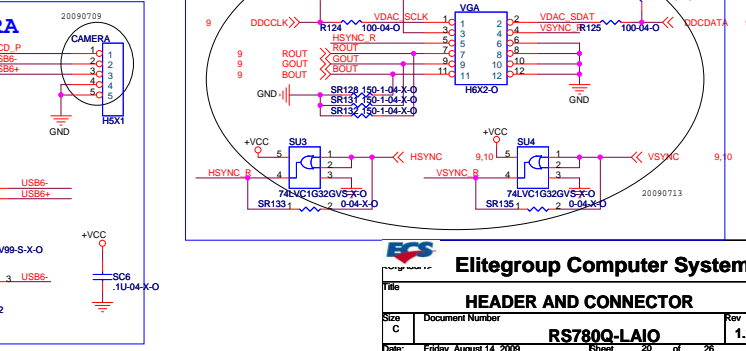
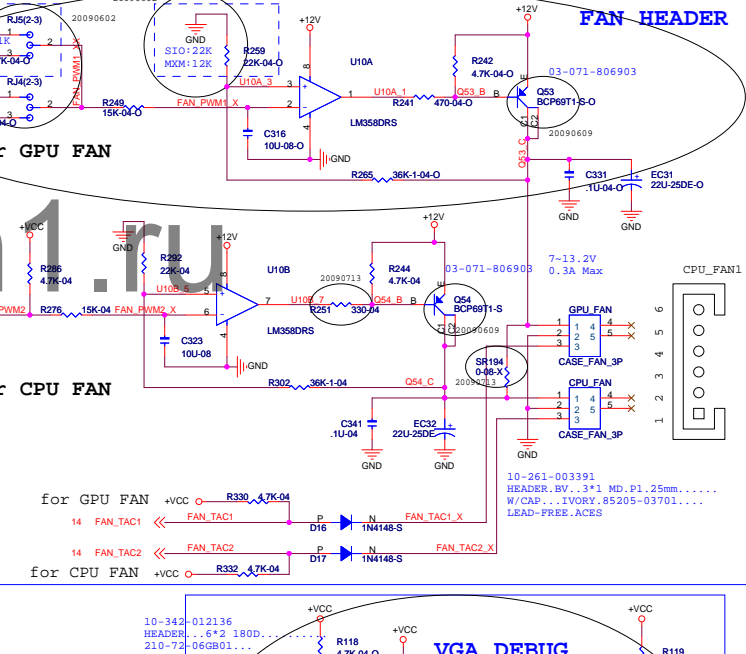
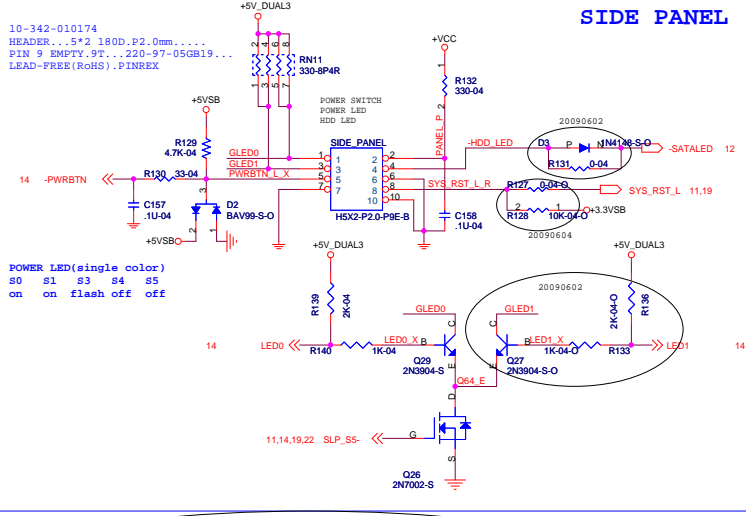
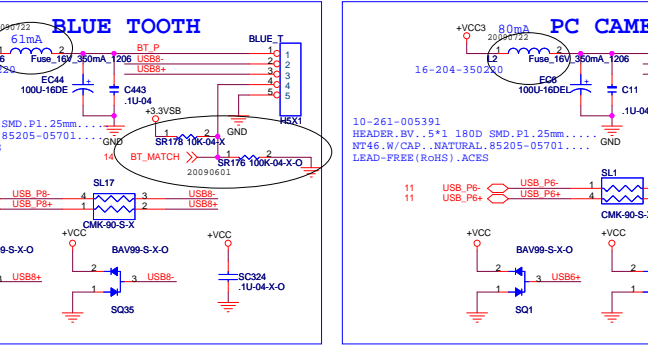
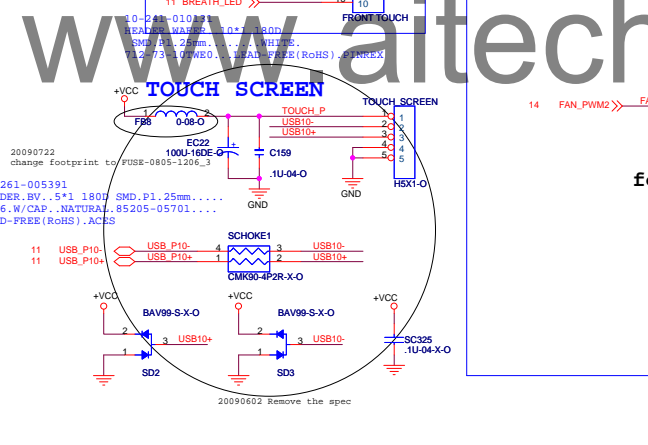
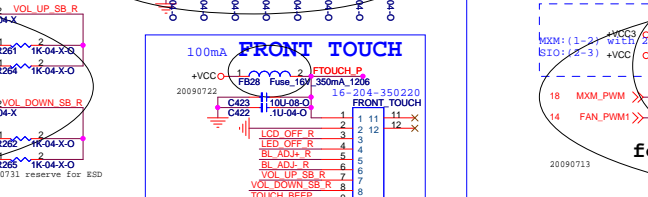
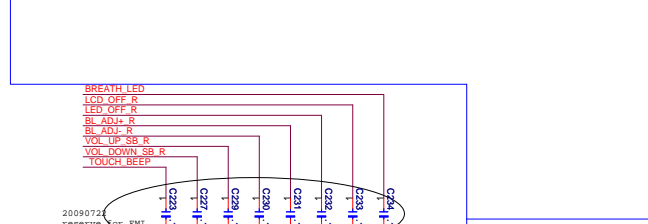
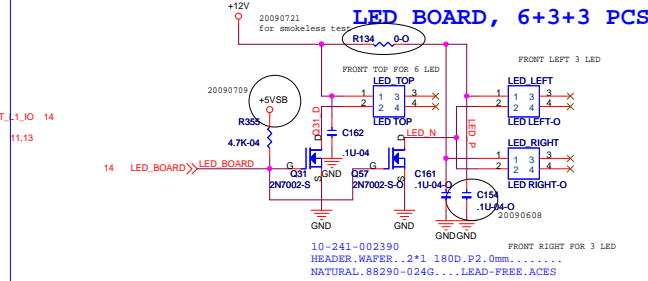
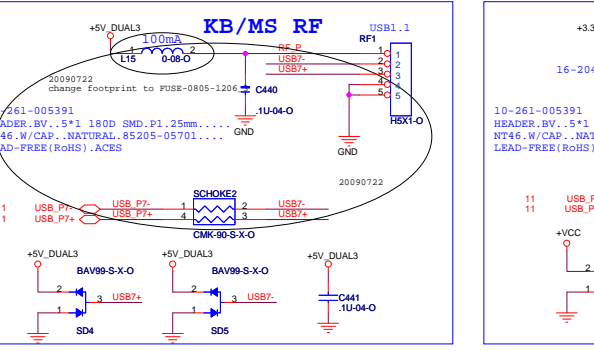
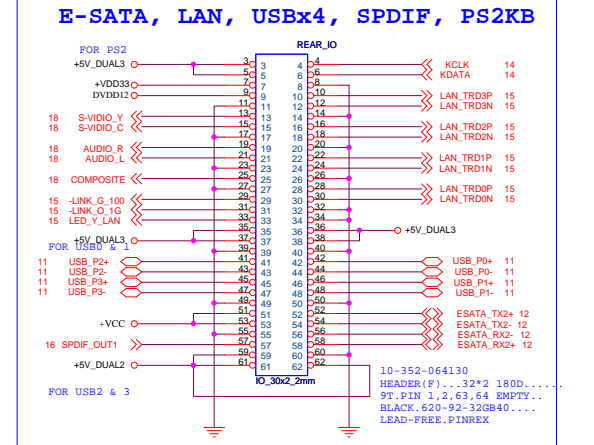
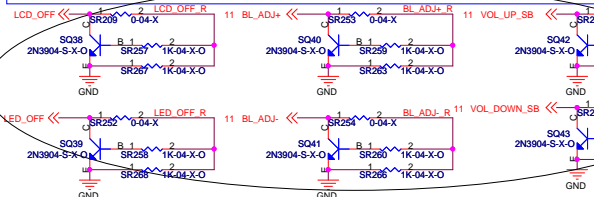
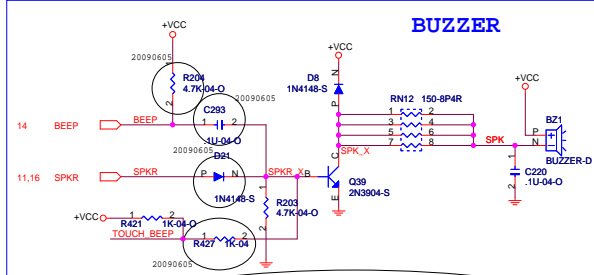
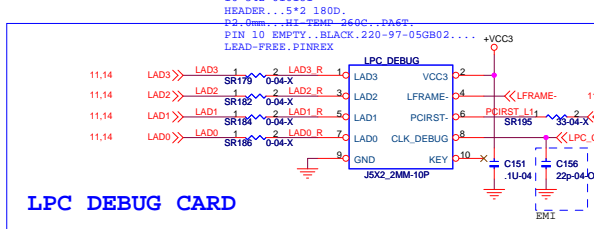






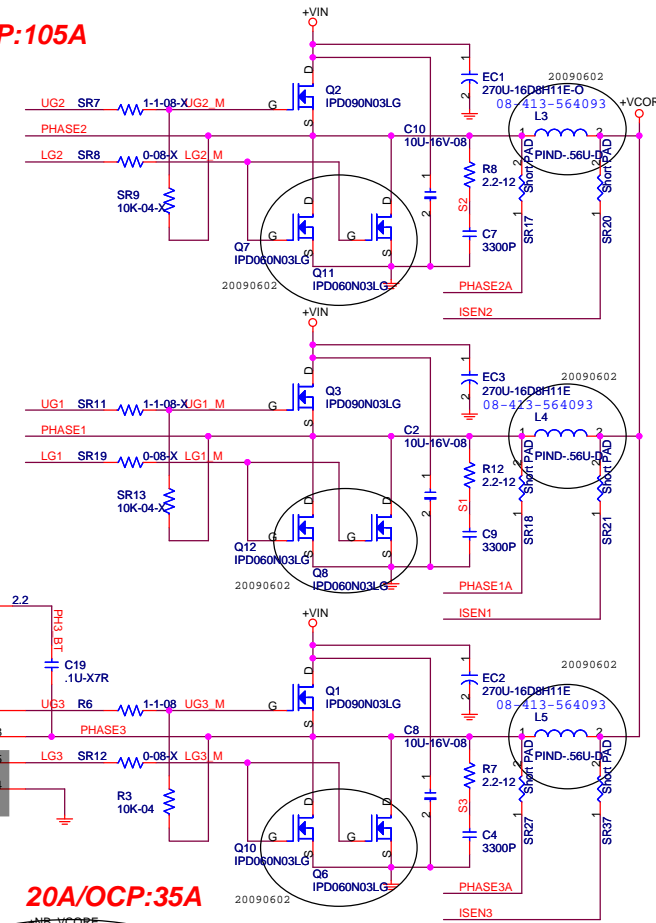




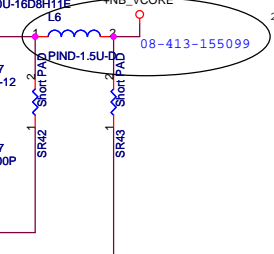




60A/OCP:105A

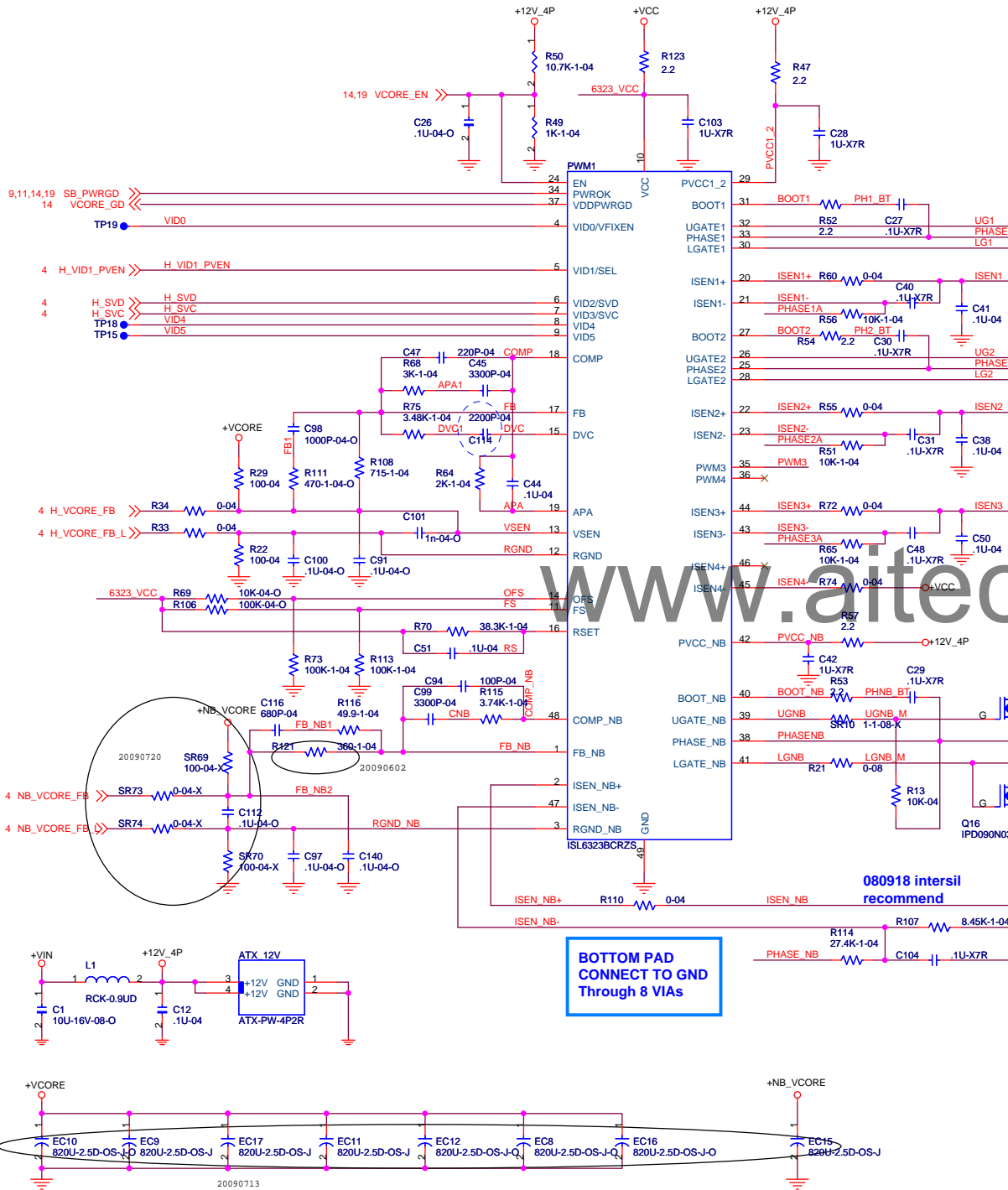


20A/OCP:35A

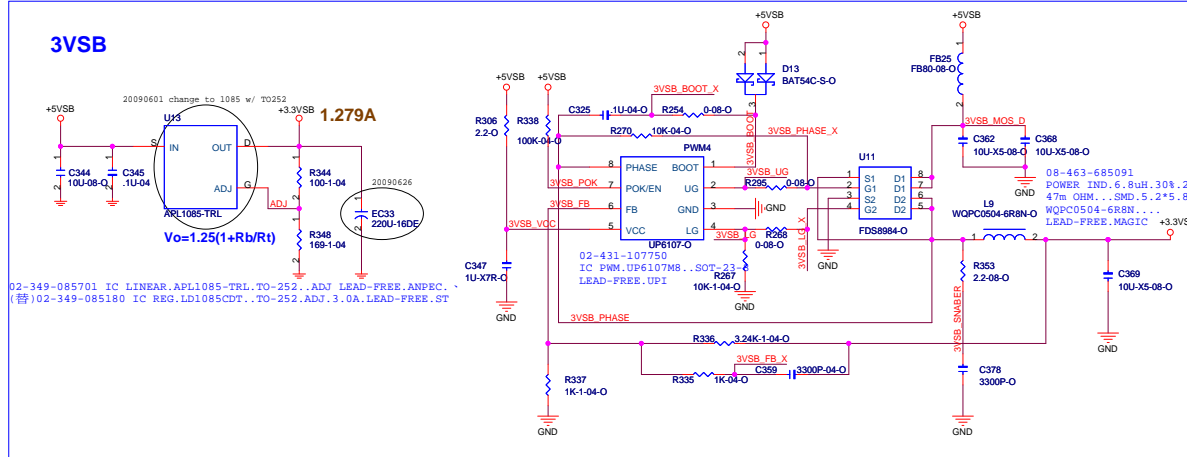


080918 intersil recommend

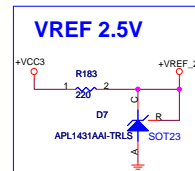
BOTTOM PAD CONNECT TO GND Through 8 Vias



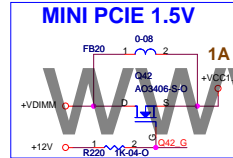
## 3VSB



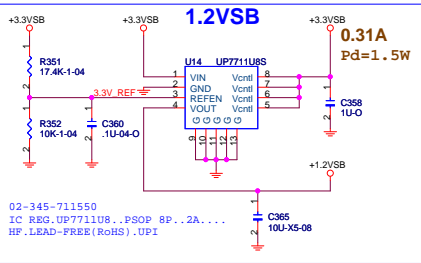
## VREF 2.5V



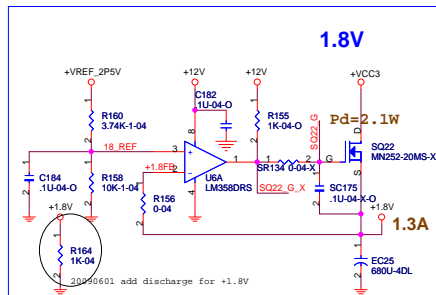
## MINI PCIE 1.5V



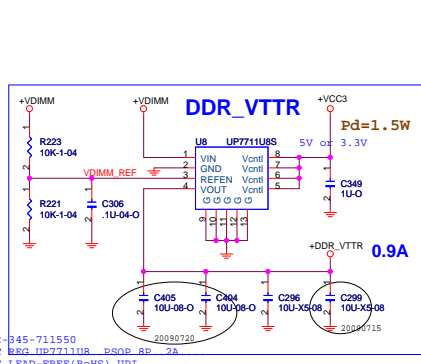
## 1.2VSB



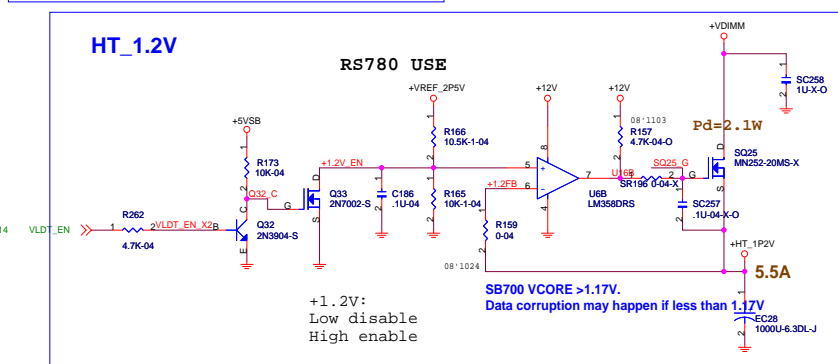
## 1.8V



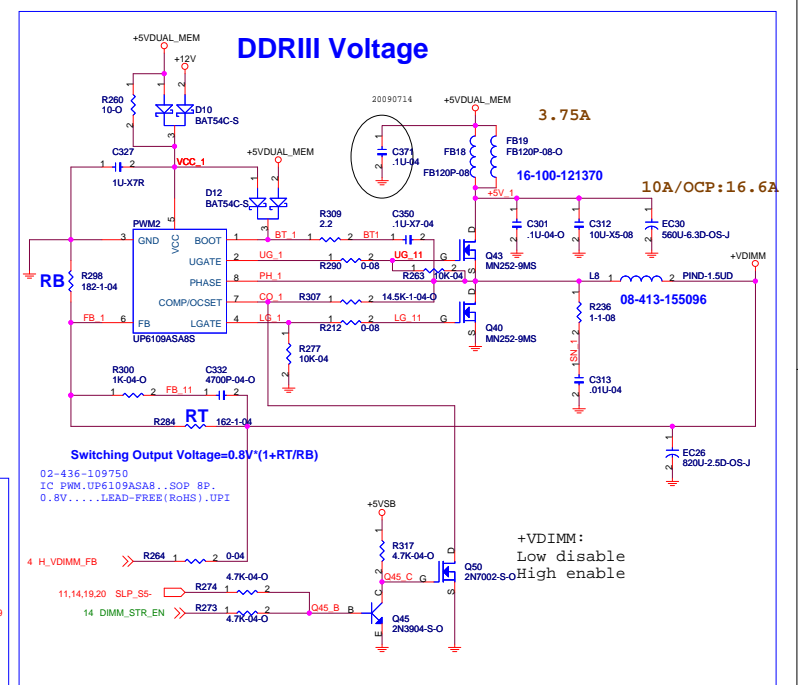
## HT\_1.2V



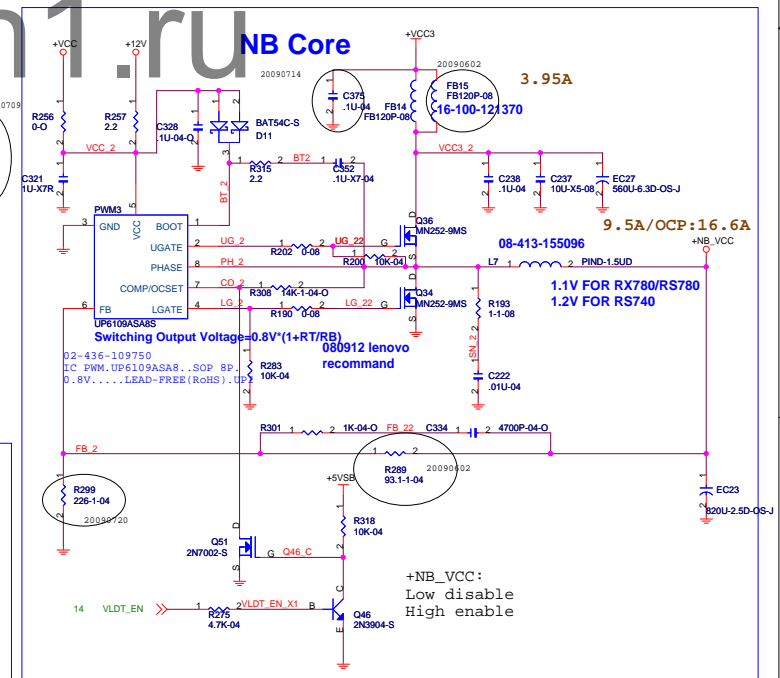
## RS780 USE

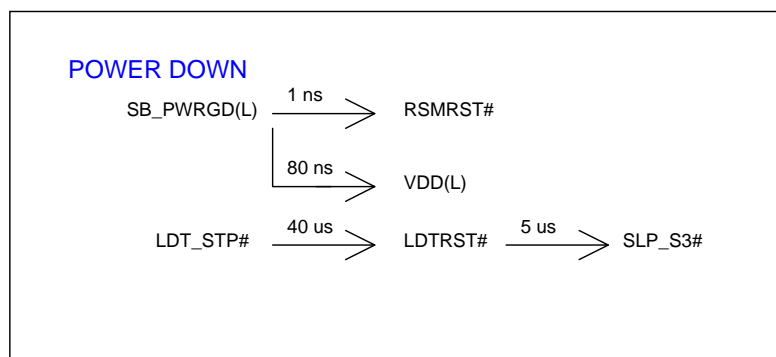
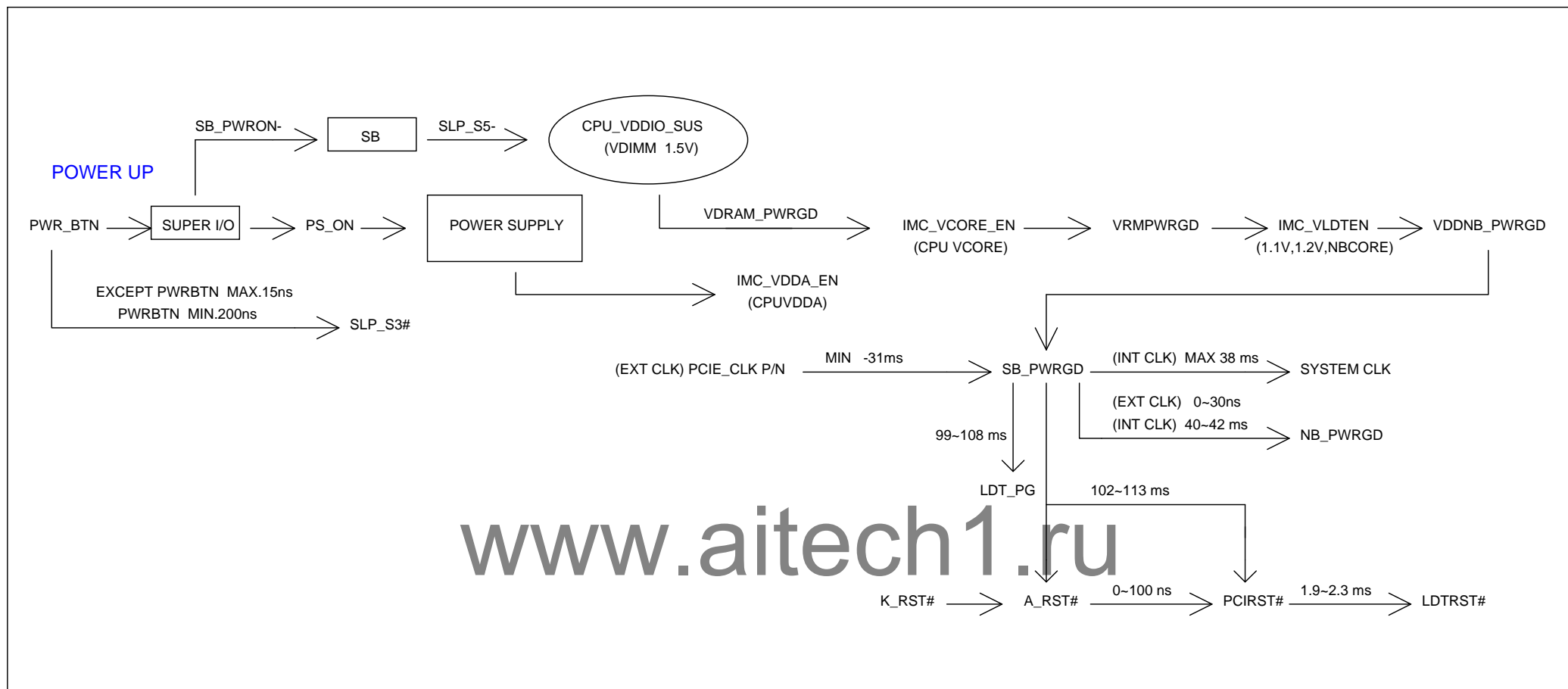


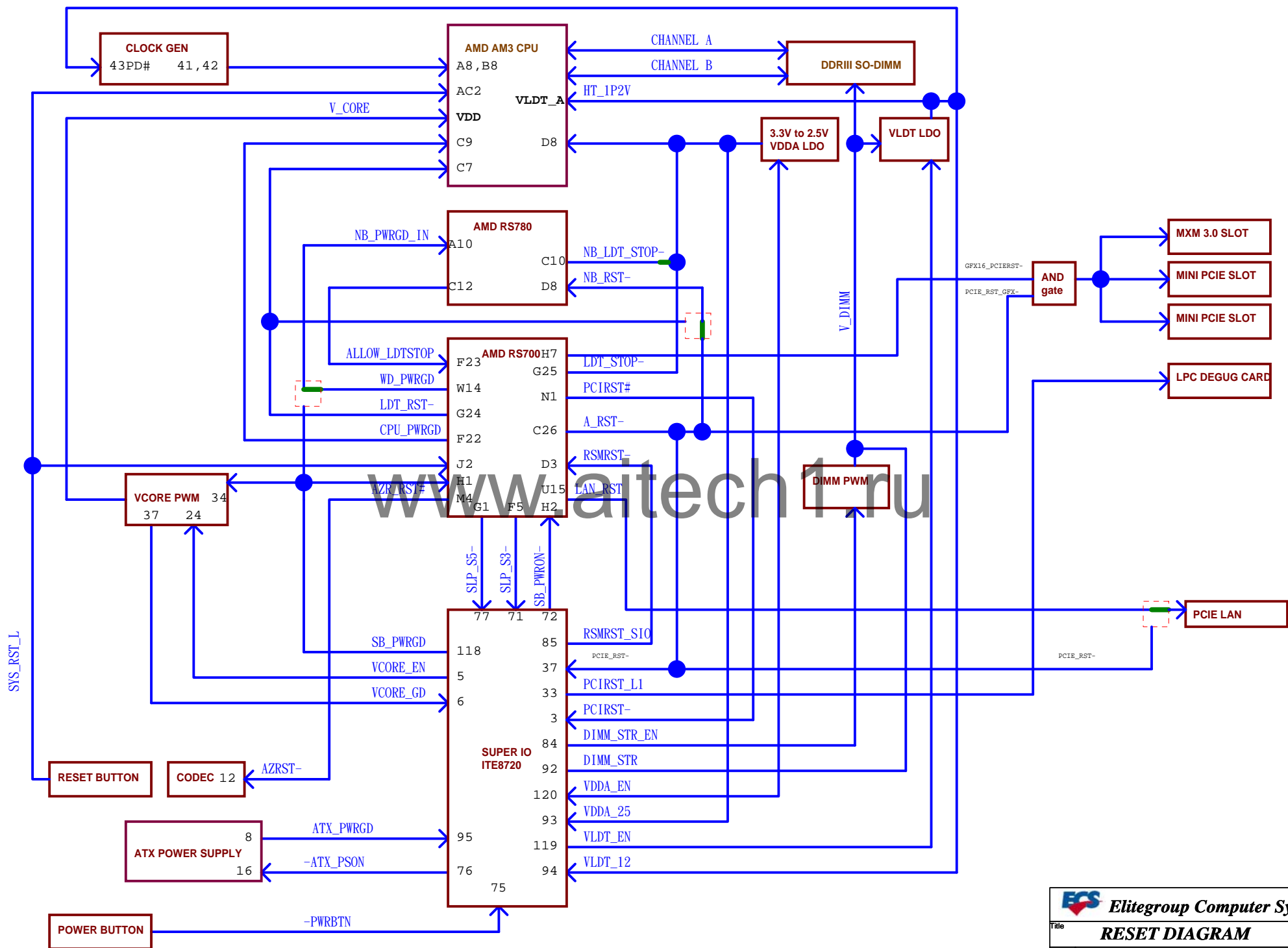
## DDR3 Voltage

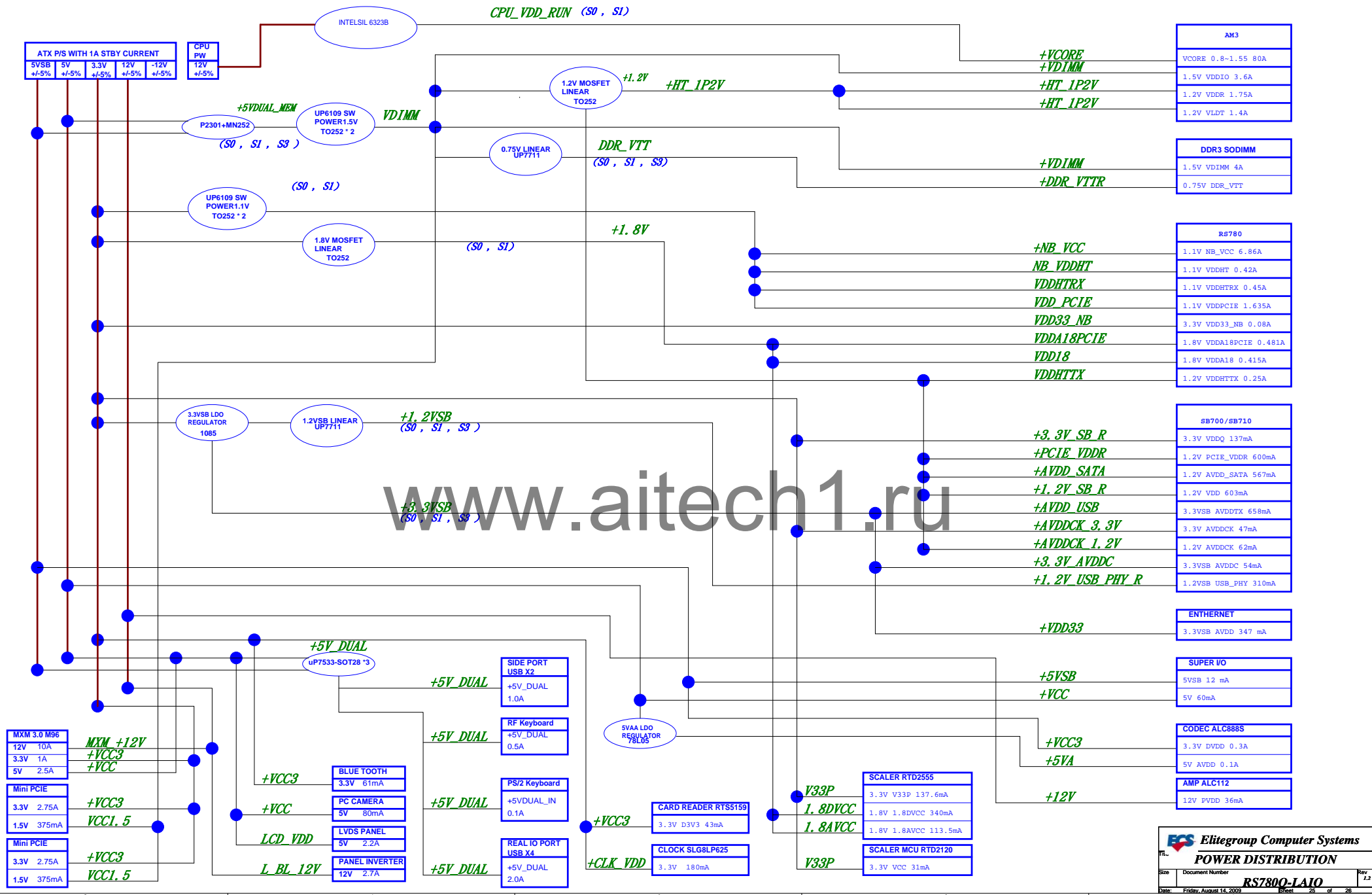


## NB Core









REVISION HISTORY:

Rev	Date	Notes	Rev	Date	Notes
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www.aitech1.ru